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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/026,813 | 12/27/2001 | Hiroo Nakano | 217781US2S | 1908 |

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| EXAMINER | |
|---|---|
| HOFFMAN, BRANDON S | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2136 | |

| NOTIFICATION DATE | DELIVERY MODE |
|---|---|
| 03/27/2008 | ELECTRONIC |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/026,813 | NAKANO, HIROO | |
| | Examiner | Art Unit | |
| | BRANDON S. HOFFMAN | 2136 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *04 January 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-4 and 11-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 11-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

1. Claims 1-4 and 11-22 are pending in this office action, claims 15-22 are newly added.

2. This action is in response to amendments file January 4, 2008, which is a response to a board decision affirming the examiner, but using a new ground of rejection. Accordingly, claims 1-4 and 11-22 are presented for examination.

3. Applicant's arguments, filed January 4, 2008, are moot in view of the new ground of rejection.

### *Claim Rejections*

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

### *Claim Rejections - 35 USC § 103*

5. Claims 1-4 and 11-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tanagawa (U.S. Patent No. 5,117,380) in view of Feyt et al. (U.S. Patent No. 6,698,662).

Regarding claims 1, 3, 11 and 13: Tanagawa discloses a data processing apparatus/memory card comprising:

- An operation processing unit (col. 2, lines 11-19, the integrated circuit) **connected to a data bus** (fig. 1, ref. num 9) **and configured to perform** a read cycle **by outputting a read control signal to a memory** (col. 2, lines 51-54) **to read a read data word output by said memory to said data bus**, and a write cycle **by outputting a write control signal to said memory and a write data word to said data bus to write said** data **word** in the **memory** (fig. 2 and col. 2, lines 40-50); and
- A pseudo-data generating circuit connected to said data bus (fig. 1, ref. num 5 and 6), **said read control signal output from said operation processing unit, and said write control signal output from said operation processing unit** (col. 2, lines 40-50), said pseudo-data generating circuit **configured to generate** pseudo-data and **output** the **generated** pseudo-data to said data bus **according to an output timing based on said read control signal and said write control signal output from said operation processing unit** (fig. 2 and col. 3, lines 8-18).

Tanagawa doesn't explicitly disclose **the output timing controlled to occur** between **a** read cycle and **an immediately following** write cycle, between **a** write cycle and **an immediately following** read cycle, between **a** read cycle **and an immediately**

**following read cycle**, or between **a** write cycle **and an immediately following write cycle**.

However Feyt et al. discloses a method for hiding operation performed by microprocessor card where he teaches presenting a random data items on the data bus during cryptographic calculation like read and write operations (col. 2, lines 36-42 and col. 3, lines 34-52).

Therefore it would have been obvious to one ordinary skilled in the art at the time the invention was made to modify the Tanagawa system with the teaching of Feyt to output pseudo-data on the data bus between read and write cycles. One would be motivated to do so in order to mask the power consumption by the memory during the reading or writing of secret data to prevent an attacker from deducing the data by correlation or differential power analysis attacks (see col. 1, lines 36-46 of Feyt et al.).

Regarding claims 2, 4, 12 and 14: Tanagawa as modified by Feyt et al. discloses wherein said pseudo-data generating circuit generates random number data as the pseudo-data (see col. 2, lines 9-19 of Tanagawa).

Regarding claims 15, 17, 19, and 21: Tanagawa as modified by Feyt et al. discloses wherein the operation processing unit is further configured to output the read control signal to have an active read control time period and an inactive read control

time period, and output the write control signal to have an active write control time period and an inactive write control time period (see col. 3, lines 19-21 of Tanagawa), and the pseudo-data generating circuit is further configured to control the output timing of the generated pseudo-data to prevent the output of the generated pseudo-data to the data bus during at least one of the active read control time period and the active write control time period (see col. 3, lines 21-26 of Tanagawa).

Regarding claims 16, 18, 20, and 22: Tanagawa as modified by Feyt et al. discloses wherein the pseudo-data generating circuit is further configured to control the output timing of the generated pseudo-data to be delayed by a predetermined time from at least one of the active read control time period and the active write control time period (see fig. 2, ref. num T2 of Tanagawa).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to BRANDON S. HOFFMAN whose telephone number is (571)272-3863. The examiner can normally be reached on M-F 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nasser G. Moazzami can be reached on 571-272-4195. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Brandon S Hoffman/
Examiner, Art Unit 2136

/Nasser G Moazzami/
Supervisory Patent Examiner, Art Unit 2136